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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/988,704	11/20/2001	Shoriki Narita	2001_1718A	9134

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EXAMINER	
CHAWAN, SHEELA C	

ART UNIT	PAPER NUMBER
2625	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/988,704	NARITA ET AL.	
	Examiner	Art Unit	
	Sheela C. Chawan	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16- 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *16, 17,25 and 26* is/are rejected.

7)☒ Claim(s) *18-23 and 26-32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on April 29, 2005 has been entered and made of record.

Claims 1-15 cancelled.

Claims 16- 32 are new.

Claims 16-32 are pending in the application.

In response to applicant's submission of a copy of substitute specification is accepted.

Response to Arguments

2. Applicant's arguments, see page 9, lines 14-16 of the remarks, filed April 29, 2005, with respect to rejection of claims 1- 15 under 103(a) have been fully considered and are persuasive. The 103(a) rejection of claims 1-15 has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Sato et al., (US 4, 929, 893).

Drawings

3. The Examiner has approved drawings filed on 11/20/01.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patent ability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claim 16,17, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata et al., (US. 6,193,132 B1), in view of Sato et al., (US.4,929,893).

As to claim 1, Shibata discloses a method for correcting ICs inclination for each of the ICs on semiconductor wafer (note, correcting IC inclination on semiconductor wafer based on two images, the first and the second image which are picked up by two cameras fig 1, element 14 and 16 and these two images are evaluated for inclination correction. The inclination correction angle is determined before the semiconductor chip is bonded, column 4, lines 12- 25, column 8, lines 1-11), comprising:

recognizing a first detection point (note, first detection point is based on the image of the lower surface, fig 1, element 15 of the semiconductor wafer before it is bonded, column 4, lines 25- 37, column 4, lines 60- 65) for recognition (column 4, lines

66-67, column 5, lines 1-12) on recognition (note, recognizing first detection point is based on the image of the lower surface, fig 1, element 15 of the semiconductor wafer before it is bonded, column 4, lines 25- 37) and a second detection point on the semiconductor wafer (note, the second detection point is obtained by the same camera from a reference point c, (column 5, lines 1-11), it also states that the measurements are taken in X and Y directions . The inclination correction is made after comparing with an image memory available, (column 6, lines 18- 21) by moving an image pickup camera along mutually orthogonal X and Y directions (note, the substrate is moved in X-axial or Y- axial direction to correct an inclination deviation, comparing with stored alignment data as shown in fig 1 does this).

Shibata is silent about specific details of correcting an inclination of all ICs on the semiconductor wafer with respect to the X and Y directions by turning the semiconductor wafer on a basis of a result of the recognition.

Sato discloses a wafer prober for use in the probe examination of semiconductor chips and wafer prober having a function for automatically aligning bonding pads of a semiconductor chip with probe needle of a probe card. The system comprises of:

loading the semiconductor wafer on a wafer turning member (fig 1, element 1, wafer chunk for holding a wafer in an X-Y stage for moving wafer chuck in X and Y directions, column 4, lines 22 – 37);

correcting an inclination of all the 1Cs on the semiconductor wafer with respect to an X- axis and a Y-axis by rotating the semiconductor wafer in a circumferential direction thereof using the wafer turning member (note, by rotating wafer chuck in a

theta direction corresponds to circumferential direction and by correcting an error in the theta direction between the wafer and the probe needle for moving wafer chuck, through X-Y stage, with an inclination of an angle corrected with respect to one of the X and Y directions, for sequential examination of plural chips on the wafer by use of the proble needle, column 11, line 21 through column 12, line 2) based on a result of said recognizing of the first detection (note, fig 1, X-axis position detector 308 corresponds to first detecting point, column 2, line 33 through column 3, line 11, column 4, lines 22-37) point and the second detection point (note, fig 1, Y-axis position detector 309 corresponds to second detecting point, column 11, lines 21-44).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Shibata to include correcting an inclination of all ICs on the semiconductor wafer with respect to the X and Y directions by turning the semiconductor wafer. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Shibata by the teaching of Sato in order to improve the alignment operation for probe needles tips which has been made manually can be made automatically, and also alignment is attainable quickly and correctly, at a constant precision, as compared with the manual alignment (as suggested by Sato column 20, lines 8- 13).

As to claims 17 and 25, Sato discloses the method wherein said correcting the inclination of all the ICs on the semiconductor wafer comprises simultaneously correcting the inclination of all the 1Cs on the semiconductor wafer (column 11, line 21 through column 12, line 2).

As to claim 24 see the rejection of claim 16.

Allowable Subject Matter

5. Claims 18-23, 26- 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact Information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheela C Chawan whose telephone number is. 571-272-7446. The examiner can normally be reached on Monday - Friday 7.30 - 4.00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh Mehta can be reached on 571-272-7453. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Sheela Chawan/

Sheela Chawan
Patent Examiner
Group Art Unit 2625
July 22, 2005